REMARKS

As a preliminary matter, applicant thanks the examiner for his indication that claims 1-9 are allowed.

Claim 11 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Go (USPN 6,320,566). Applicant traverses this rejection because the cited prior art reference does not disclose (or suggest) a timing controller that outputs data signals of even-numbered dots and data signals of odd-numbered dots, while displacing the phase of the data signals of even-numbered dots and odd-numbered dots by 180 degrees.

Go is directed to a driving circuit for a liquid crystal display, and discloses a controller integrated circuit (IC), which the examiner asserts corresponds to the timing controller of present claim 11. The controller IC generates a first clock signal FD1 and a second clock signal FD2, where the second clock signal FD2 is 180° different than the first clock signal FD1. As shown in Fig. 10 of Go, the controller IC 100 also provides, as outputs, video signals S1 and S2. However, as shown in Fig. 11, Signals S1 and S2 are in phase with one another.

In contrast, the present application teaches that a timing controller outputs data signals of even-numbered dots while shifting the phase by 180° relative to data signals of odd-numbered dots. Since Go fails to disclose a timing controller that produces video signals that are out of phase with respect to one another, as recited in claim 11, withdrawal of the rejection of claim 11 is respectfully requested.

Claim 10 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Go in view of Jeong (USPN 6,335,721). Applicant traverses this rejection because the cited references, taken alone or in combination, fail to disclose or suggest selecting a first or second clock signal based on a selection signal, and selectively latching data signals with the first or second clock signal.

Go is directed to a driving circuit for a liquid crystal display. The reference discloses a data driver integrated circuit that receives a first clock signal FD1 and a second clock signal FD2 as inputs, where the second clock signal FD2 is 180° out of phase with the first clock signal FD1. However, as acknowledged by the examiner, Go fails to disclose selecting the first or the second clock signal based on a selection signal. Go further fails to disclose selectively latching data signals with the first or second clock signal. Instead, the examiner relies on Jeong to disclose these features.

Jeong shows, in Fig. 5, control logic used to determine an output video signal. Input video signals are first routed through a latch 101, which latches data based on a clock signal CLK1. From there, data is routed to an EVEN input of a multiplexer 105 through a second latch 102, which latches data based on an input clock signal CLK2. Data is routed to an ODD input of the multiplexer 105 through a pair of latches latches 103 and 104, where the latch 103 latches data based on the clock signal CLK1 and the latch 104 latches data based on the clock signal CLK2. That is, immediately prior to being input to the multiplexer 105, both the EVEN data and the ODD data pass through latches 102 and 104 respectively, which both latch data based on clock signal CLK2. Finally, one of the EVEN data and the ODD

data is selected based on an internal polarity control signal POL_INT. Thus, Jeong teaches that the input POL_INT is used for selection of video signal data, and not selection of a first or second clock signal, as recited in the present claims.

Further, both the EVEN data and the ODD data are latched with the second clock signal when the multiplexer receives the signals as inputs. Also, as is clear from Fig. 5 of Jeong, the data input to both the EVEN and ODD inputs of the multiplexer are latched with both the first clock signal CLK1 and the second clock signal CLK2 before being output from the control logic. Thus, Jeong also fails to disclose selectively latching data signals with the first or second clock, as recited in claim 10 of the present application.

Accordingly, since Go and Jeong, taken alone or in combination, fail to disclose or suggest selecting a first or second clock signal based on a selection signal, and selectively latching data signals with the first or second clock signal, applicant respectfully requests withdrawal of the rejection of claim 10.

Claim 12 stands rejected under § 103(a) as being unpatentable over Go in view of Ogata et al. (JP 407329337). Applicant traverses the rejection because the cited references, taken alone or in combination, fail to disclose or suggest arranging data signal output pins in a timing controller so that the data signal of an odd-number dot of each bit of each color and the data signal of an even-number dot of the same bit are directly adjacent to each other.

The examiner acknowledges that Go fails to disclose that a data signal of a dot includes a plurality of bits, and that output pins for data signals are arranged so that the data

signal of an odd-number dot of each bit of each color and the data signal of an even-number dot of the same bit are directly adjacent to each other, and instead relies on Ogata to disclose these features.

Ogata shows, in Fig. 1, that odd-numbered data lines 1, 3, ..., n-1 are output from shift register 21, and even-numbered data lines 2, 4, ..., n are output from shift register 22. The examiner asserts that line 1 through n correspond to dots 1 through n in a line of a display. Further, the examiner asserts that because shift register 21 and shift register 22 are shown as adjacent in Fig. 1, that the output pin for one bit of an odd-numbered dot is adjacent to the output pin of the same bit of an even-numbered dot, as recited in the present specification. However, as the examiner correctly points out, odd-numbered data lines and even-numbered data lines pass through distinct shift registers. Accordingly, it is clear that the output pin for one bit of an odd-numbered dot is not directly adjacent to the output pin of the same bit of an even-numbered dot, as recited in the present claims.

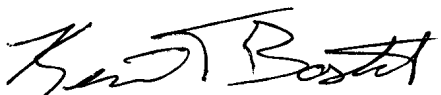
In contrast, the present application teaches that a dot is made up of 3 colors, and that each of those colors is specified using 8 bits numbered 0 through 7. Bits are identified according to color, bit number, and whether a dot is even or odd. For example, the first bit of the red color portion of an odd dot is referred to as R0O, while the first bit of the red color portion of an even dot is referred to as R0E. Fig 15 of the present application shows an arrangement of the output pins of a timing controller 108. It is clear from the figure that for each output pin of an odd dot, a corresponding output pin of an even dot is adjacent thereto. For example, the output pin for bit R7E is directly adjacent to the output

pin for bit R7O, the output pin for bit G0E is directly adjacent to the output pin for bit G0O, and so on. Because Go and Ogata, taken alone or in combination, do not disclose this configuration, applicant requests withdrawal of the rejection of claim 12.

For all of the foregoing reasons, applicant submits that this application is in condition for allowance, which is respectfully requested. The examiner is invited to contact the undersigned attorney if an interview would expedite prosecution.

Respectfully submitted,

GREER, BURNS & CRAIN, LTD.

By 
Kevin T. Bastuba
Registration No. 59,905

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300 South Wacker Drive
Suite 2500
Chicago, Illinois 60606
Telephone: 312.360.0080
Facsimile: 312.360.9315

Customer No. 24978